

20250414 041709

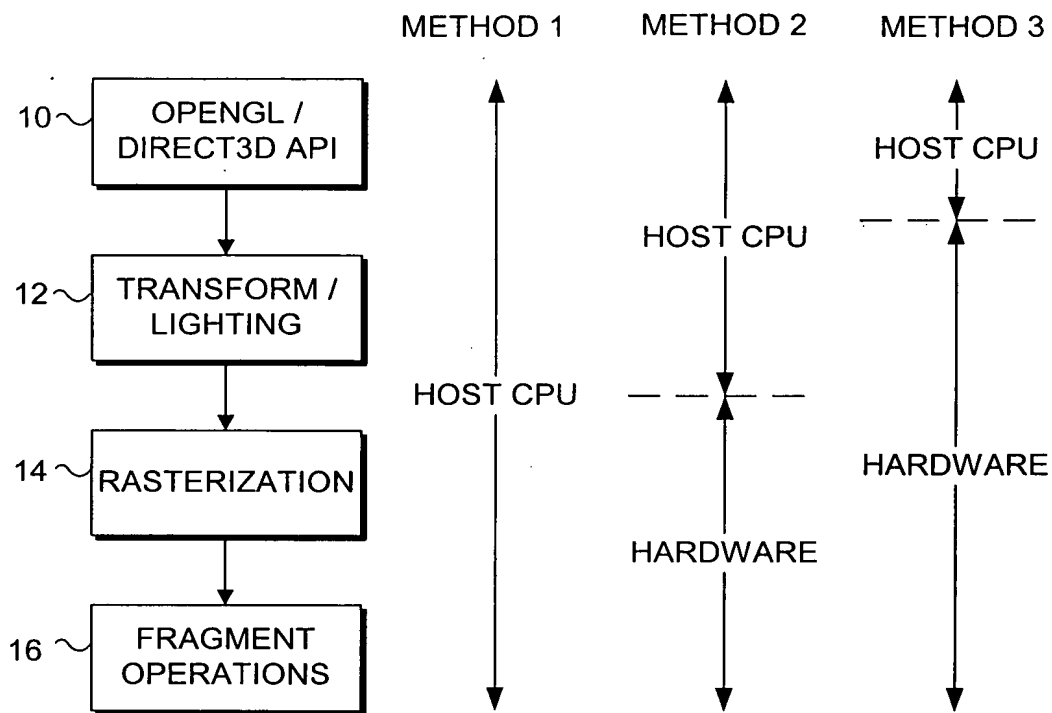


FIG. 1

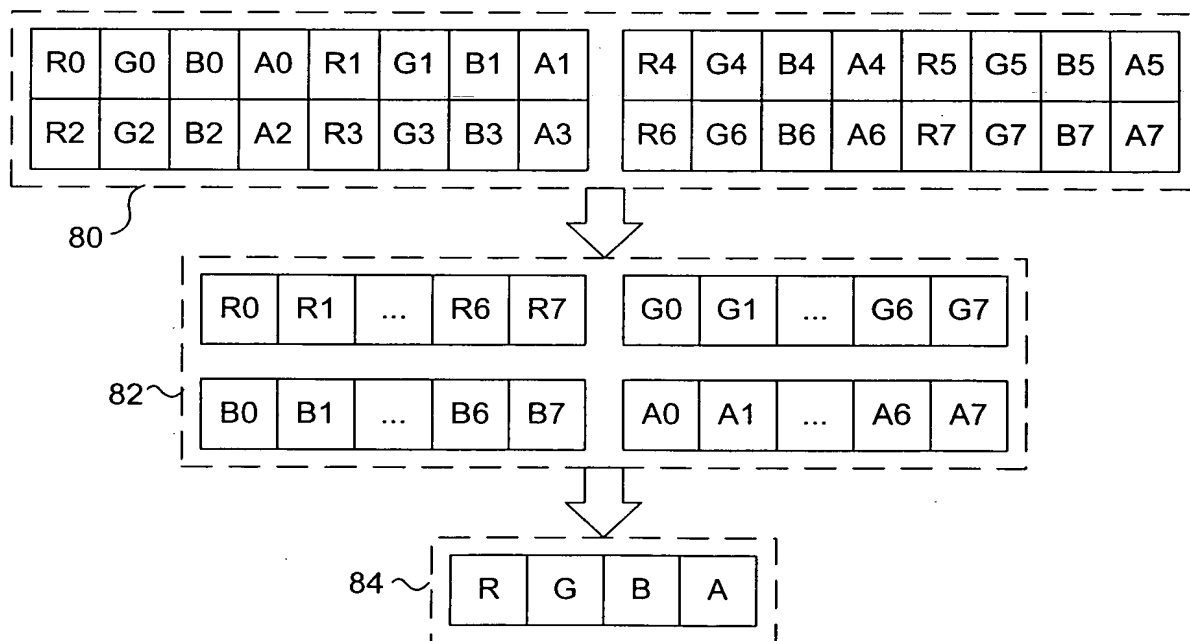


FIG. 4

```

graph TD
    CPU[HOST CPU 18] --> Config[CONFIG REGS 19]
    CPU --> RU[RASTERIZATION UNIT 22]
    Config --> RU
    Config --> ZBU[Z-BUFFER UNIT 24]
    Config --> TAU[TEXTURE ADDRESS UNIT 26]
    Config --> TC[TEXTURE CACHE 28]
    Config --> TFU[TEXTURE FILTERING UNIT 30]
    Config --> BU[BLENDING UNIT 32]
    
    RU --> ZBU
    ZBU --> TAU
    TAU --> TC
    TC --> TFU
    TFU --> BU
    BU --> MC[MEMORY CONTROLLER 34]
    MC --> MEM[MEMORY 36]
    
    subgraph 20 [ ]
        subgraph 14 [RASTERIZATION]
            RU
        end
        subgraph 16 [FRAGMENT OPERATIONS]
            ZBU
            TAU
            TC
            TFU
            BU
        end
    end

```

(PRIOR ART)

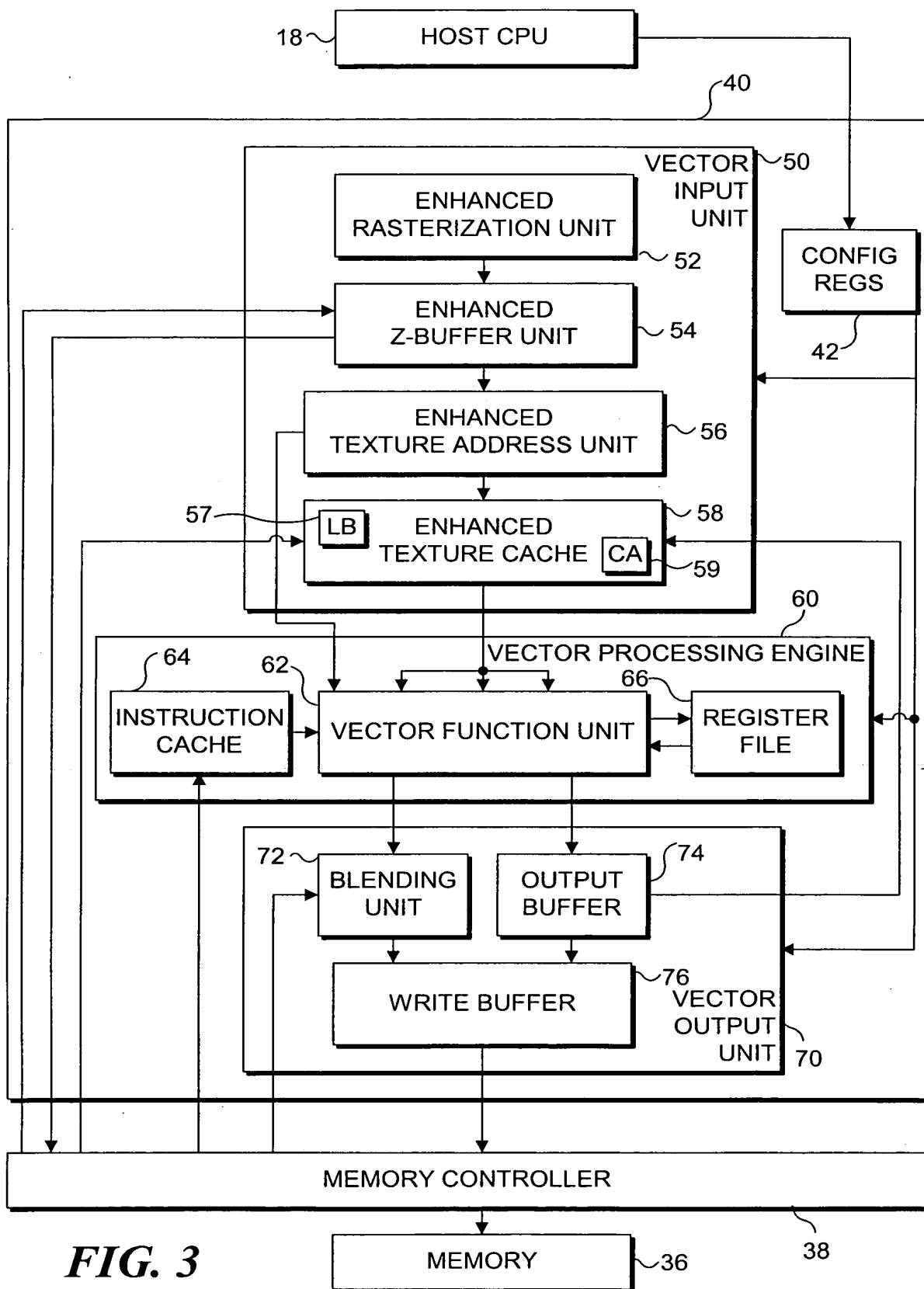


FIG. 3

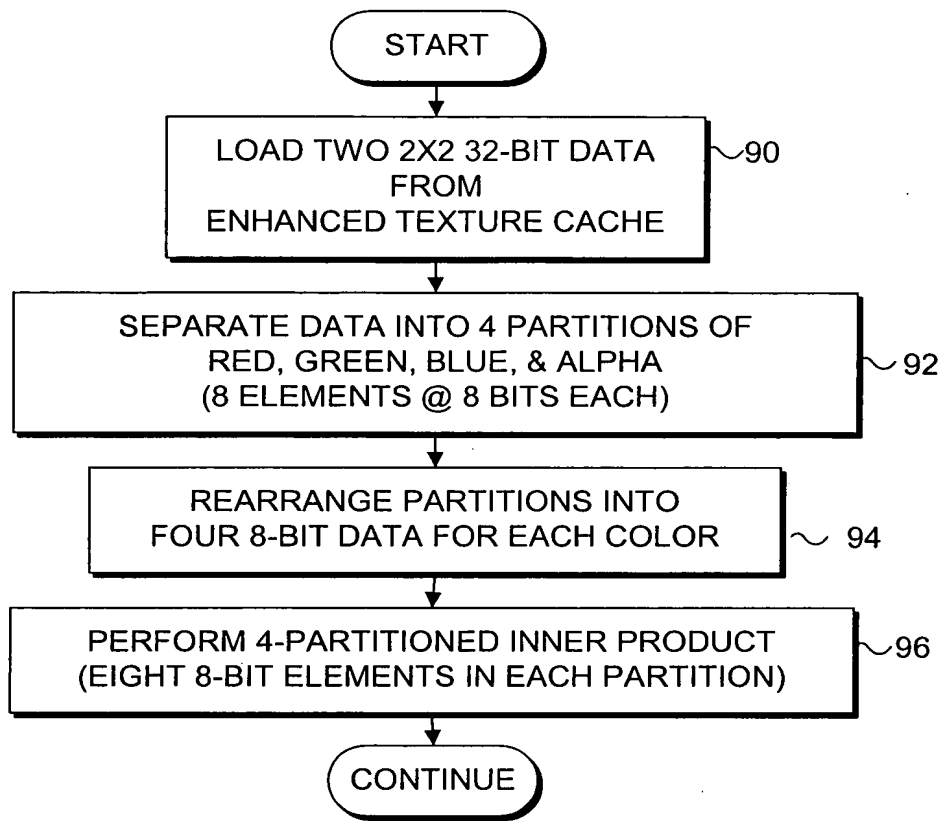
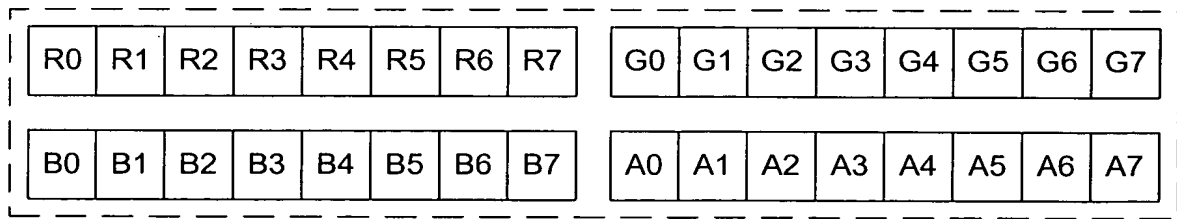
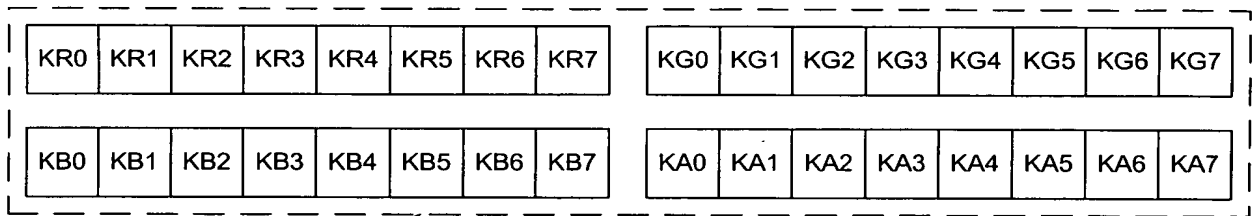


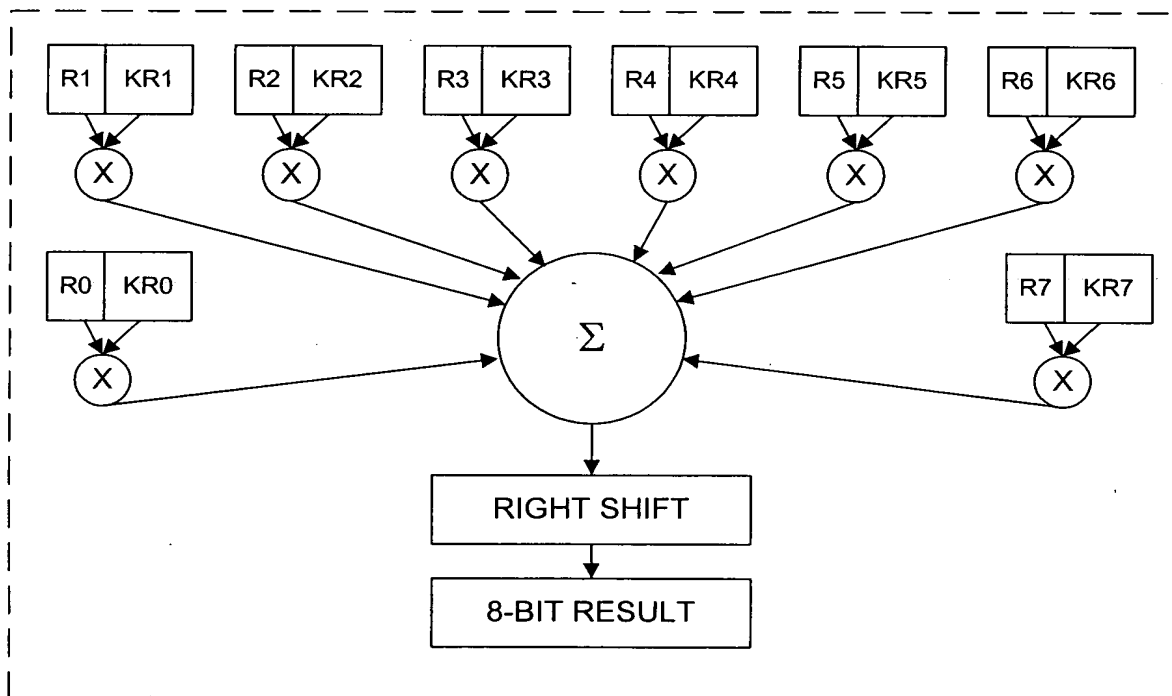
FIG. 5



100

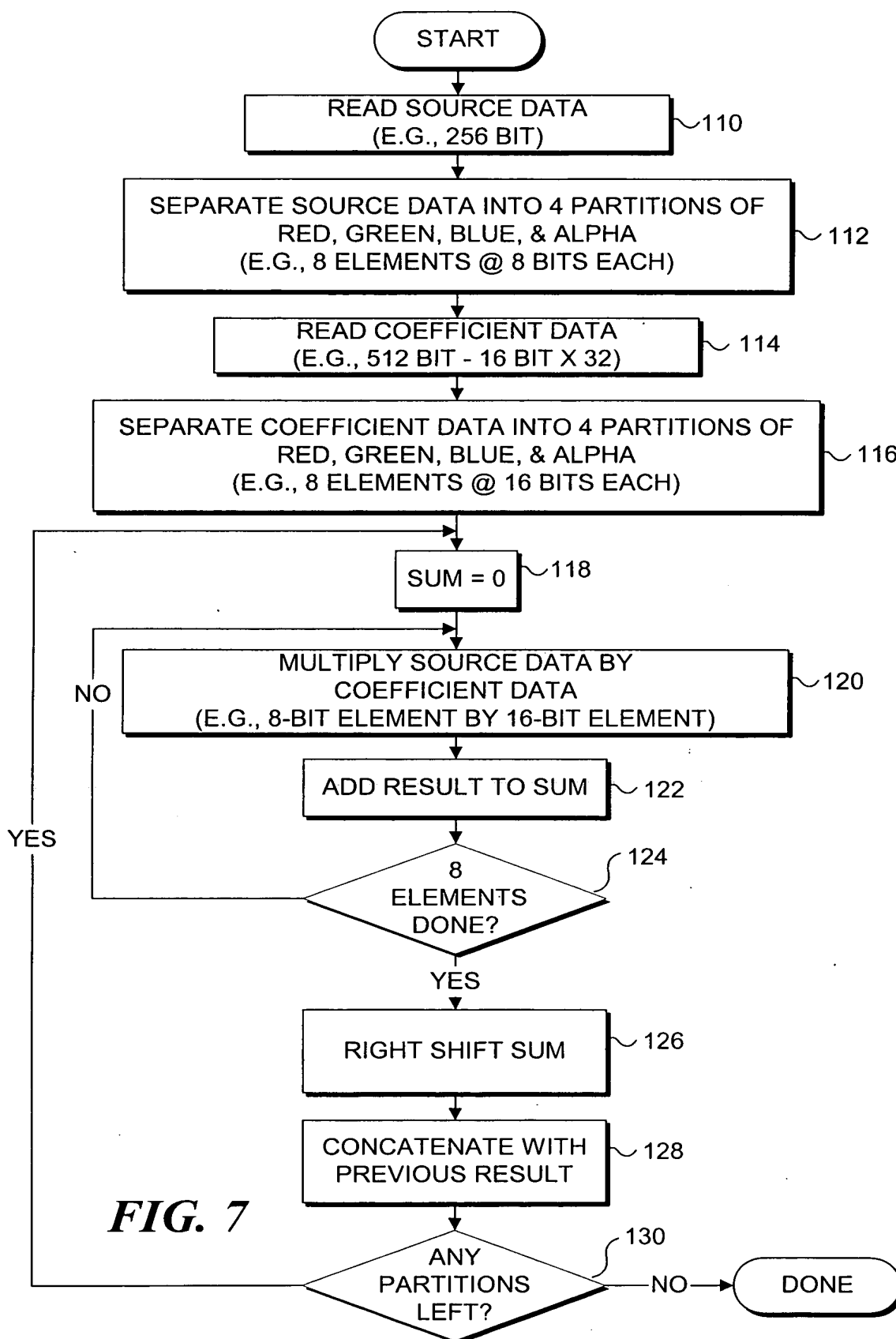


102



104

FIG. 6



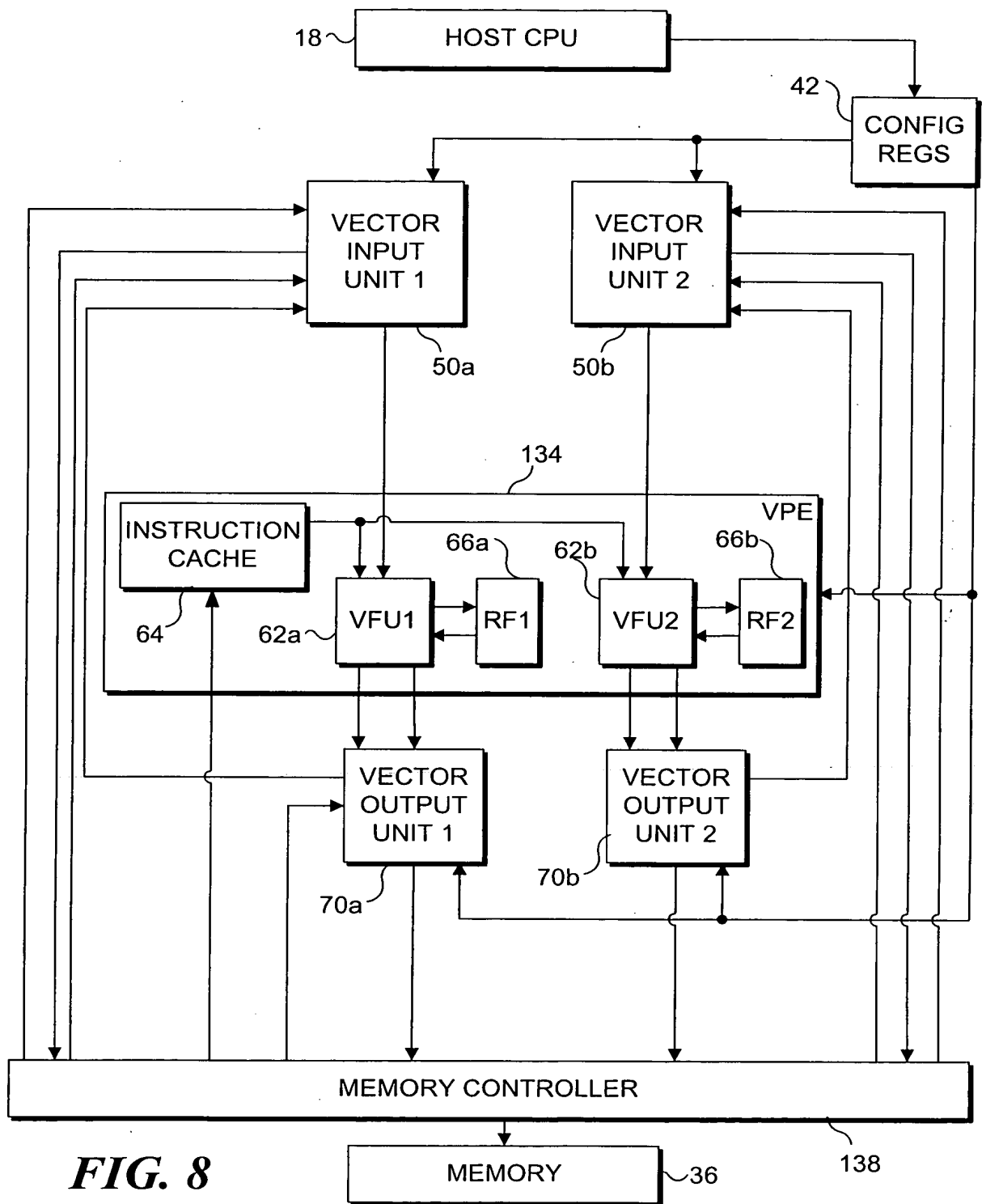
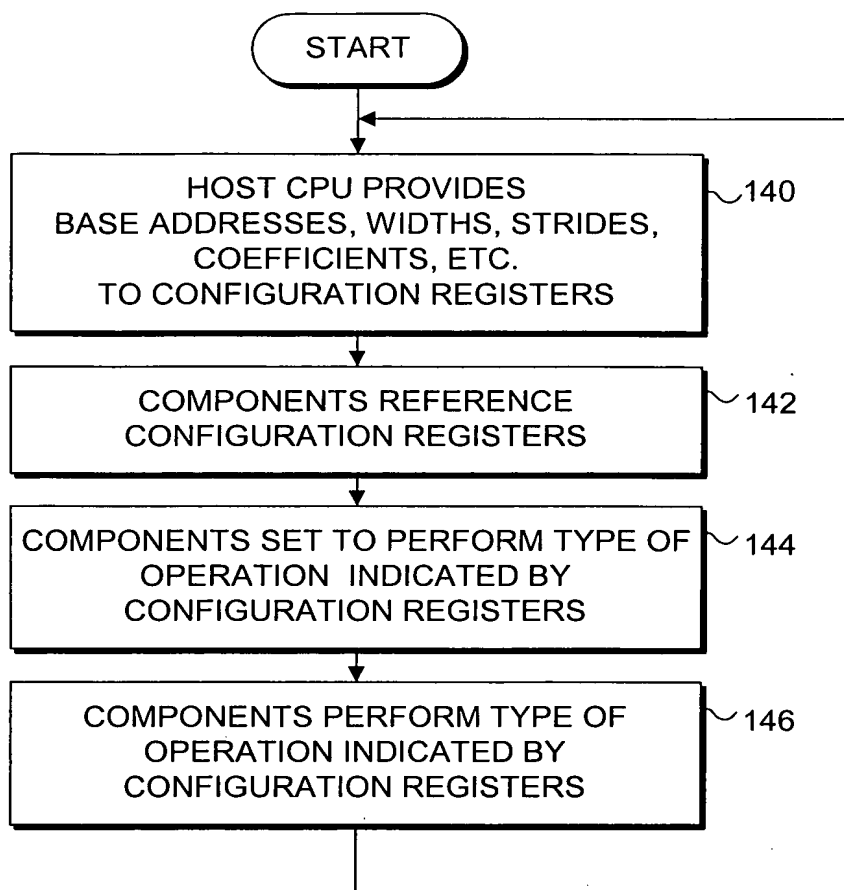


FIG. 8

**FIG. 9**

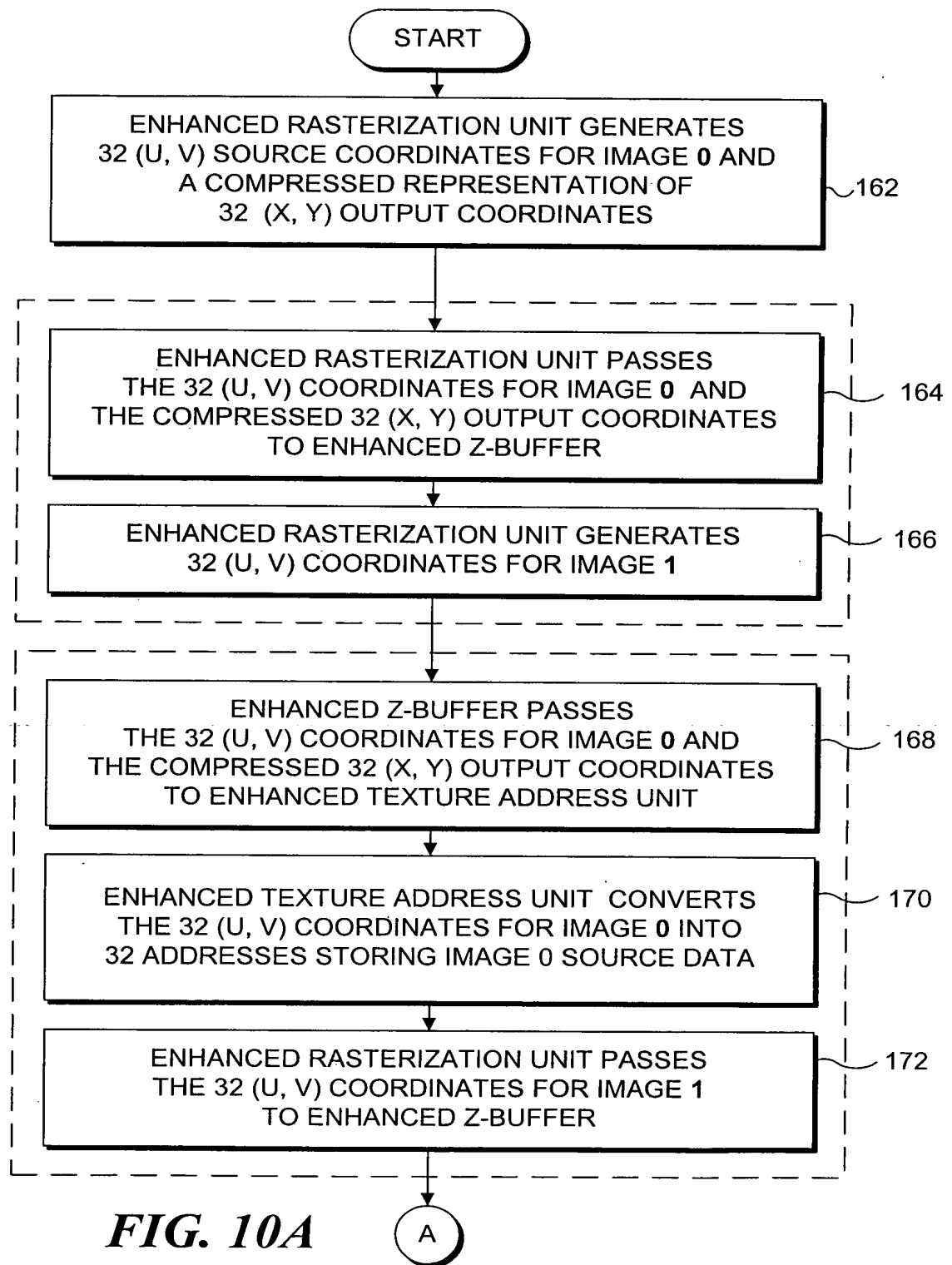


FIG. 10A

2025 RELEASE UNDER E.O. 14176

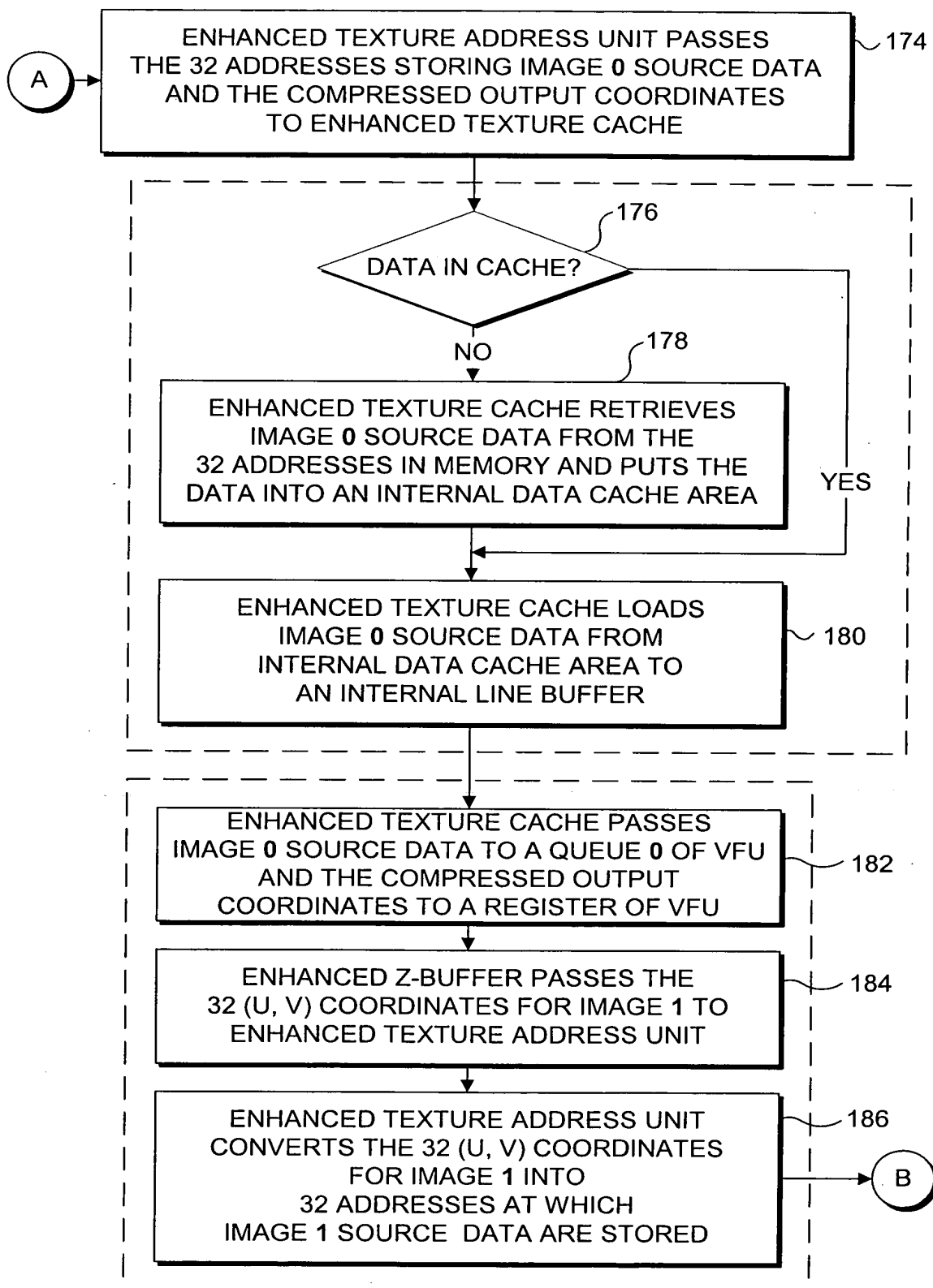


FIG. 10B

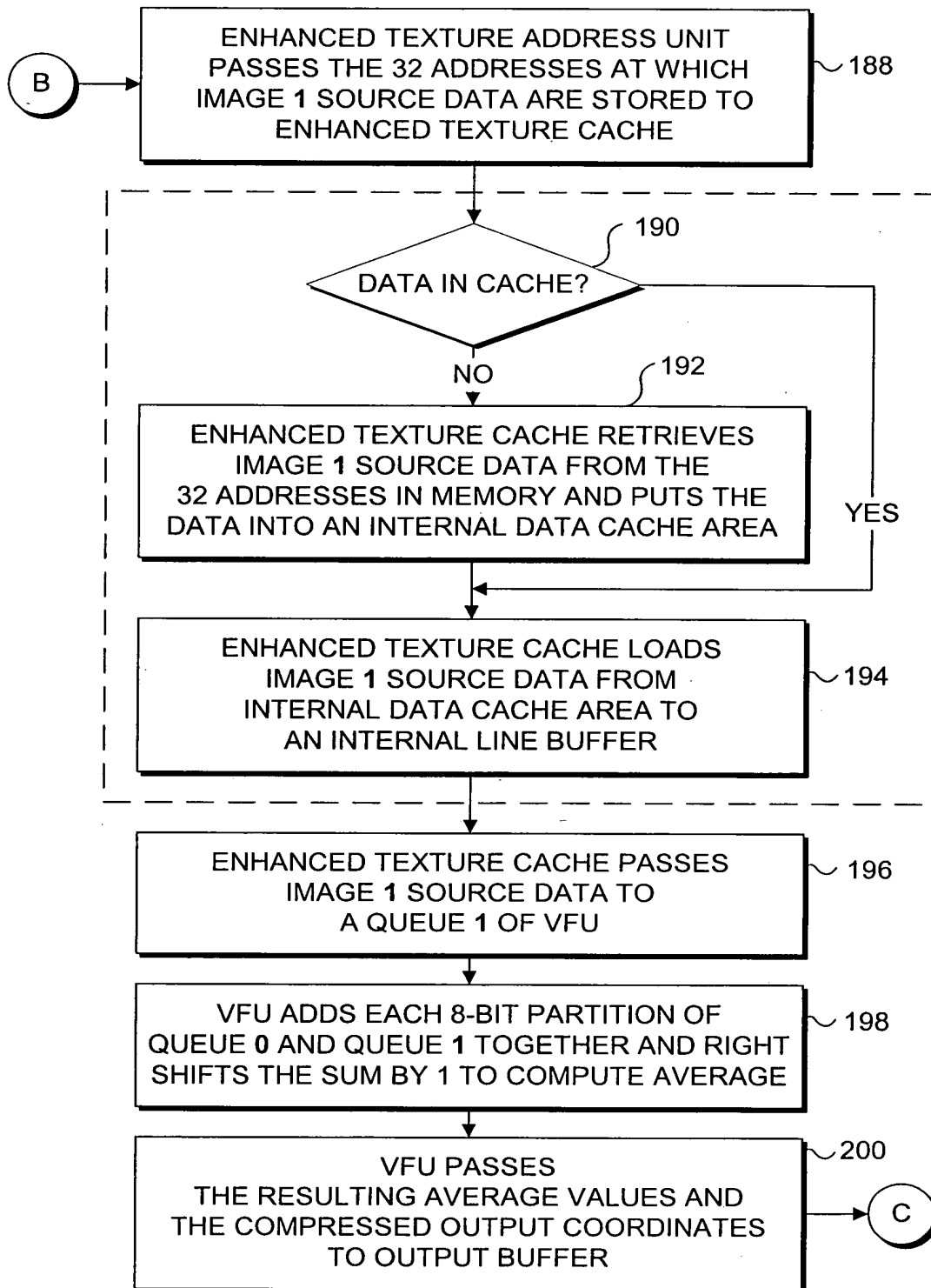


FIG. 10C

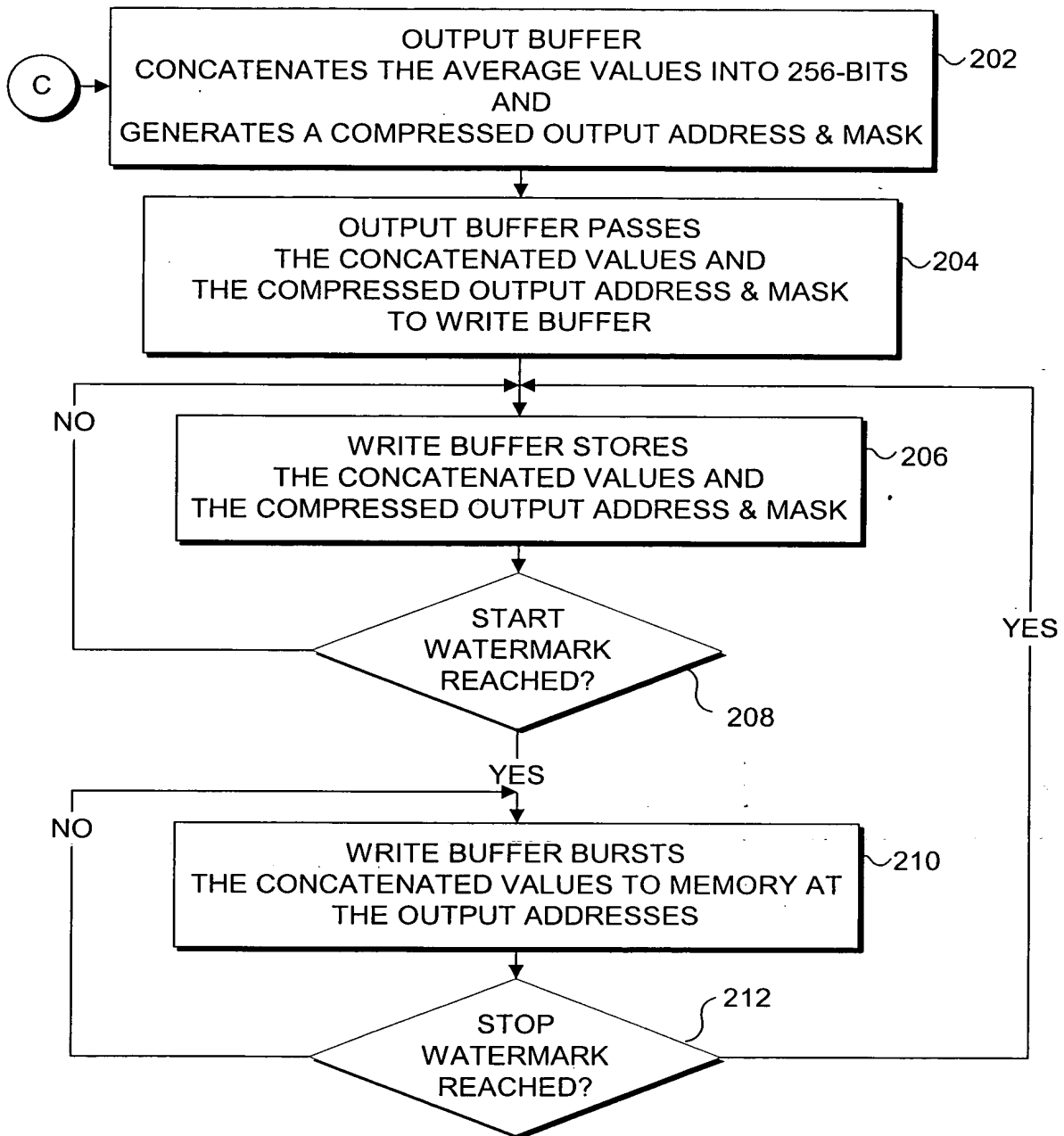


FIG. 10D

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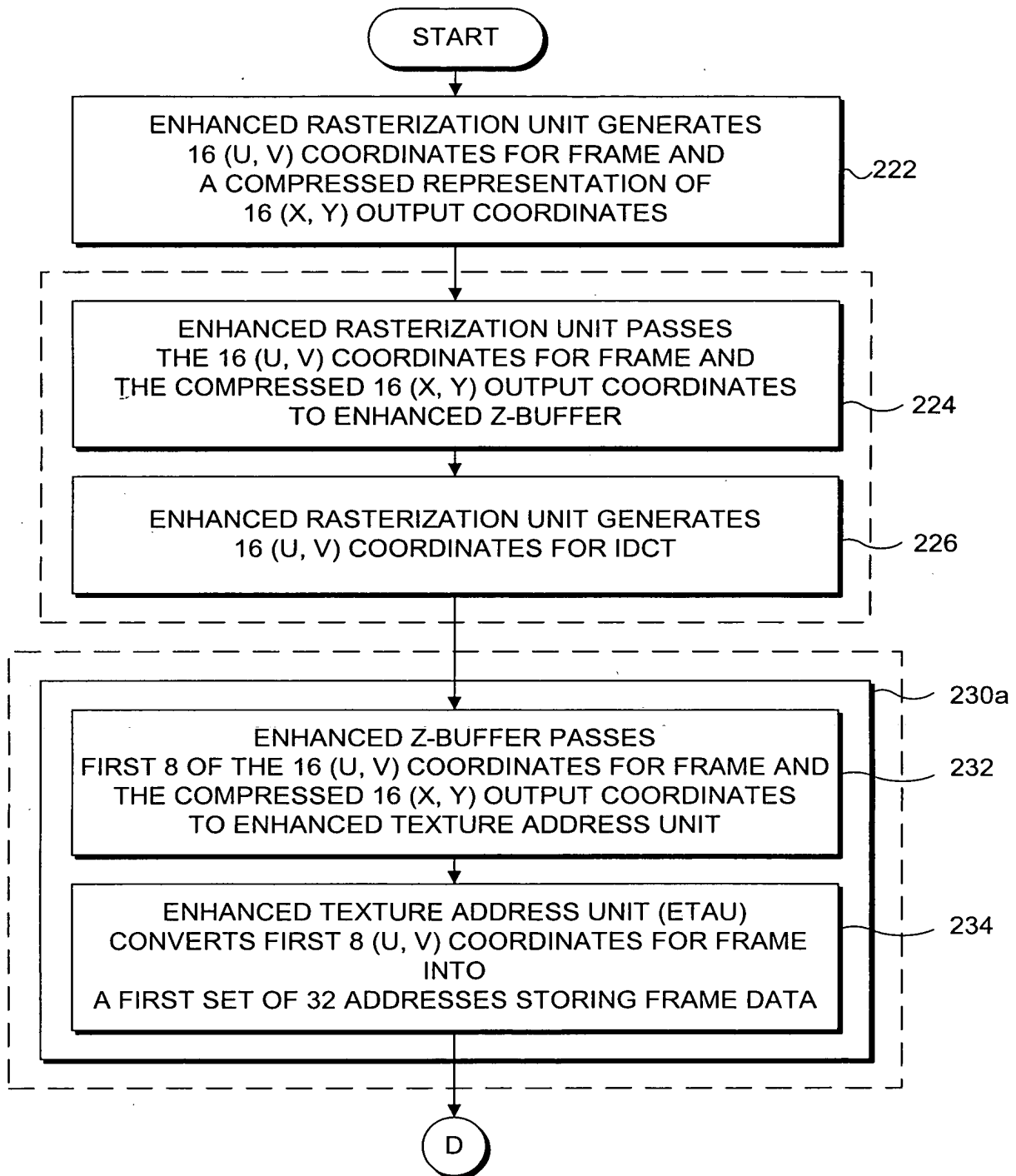


FIG. 11A

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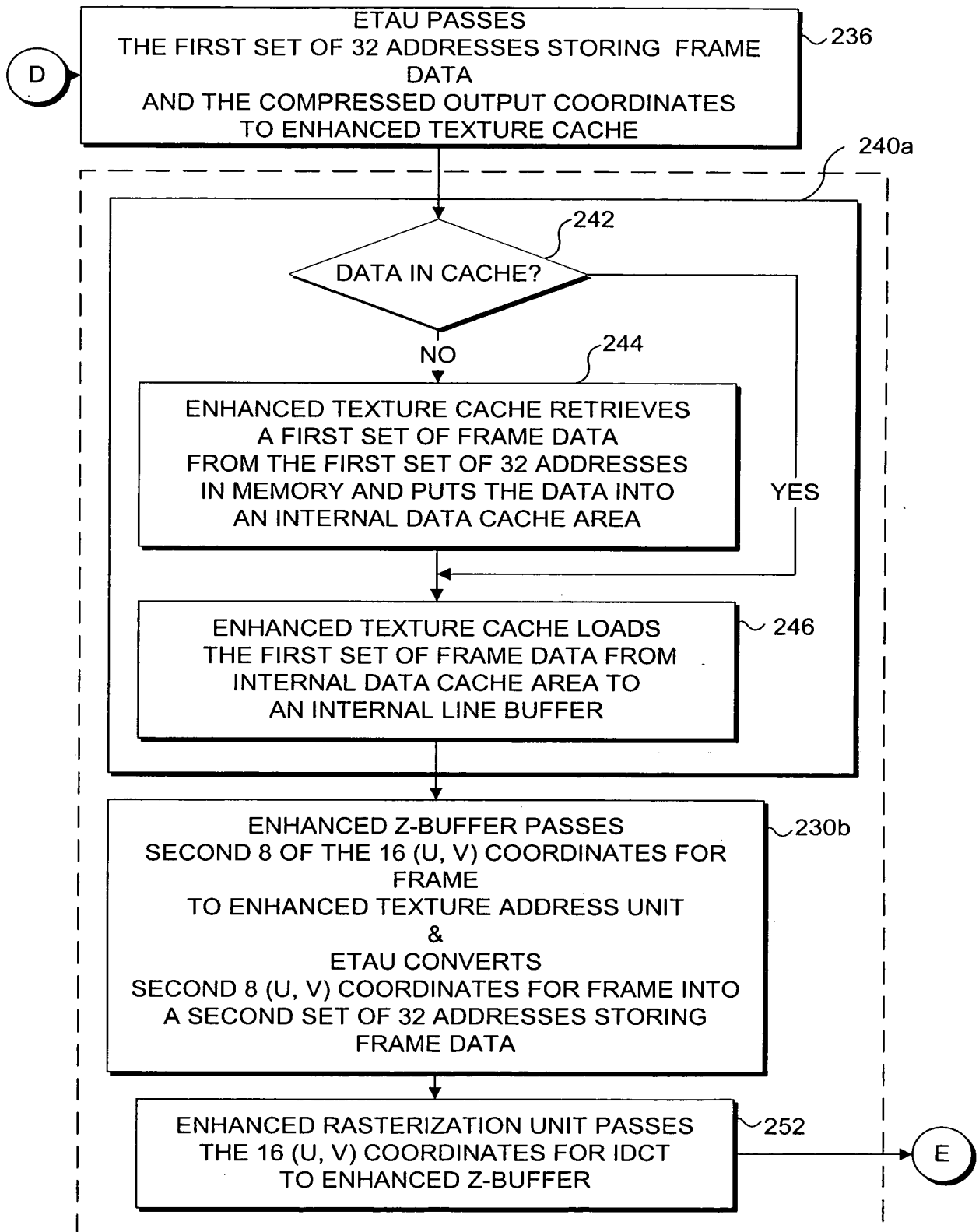


FIG. 11B

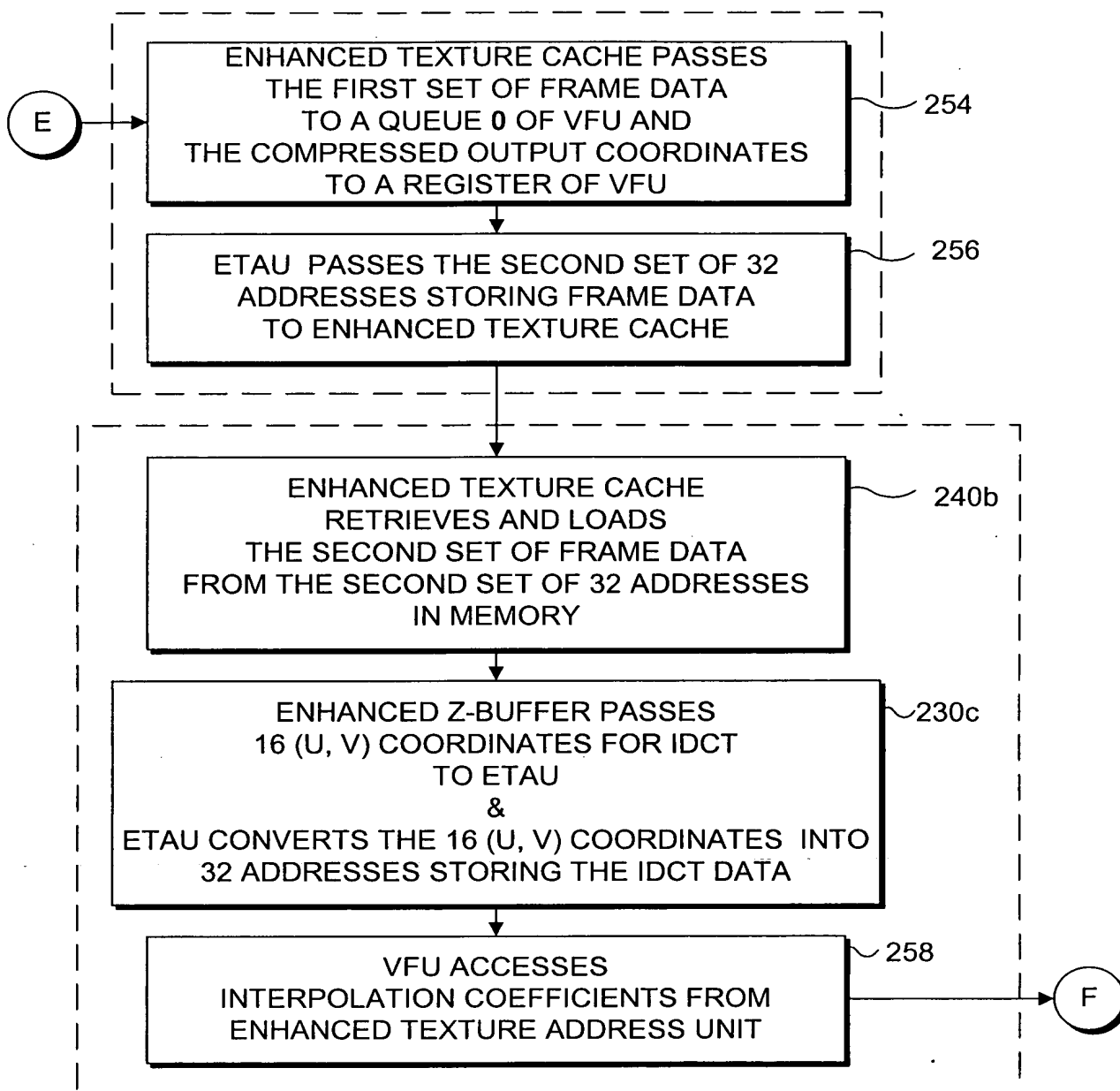


FIG. 11C

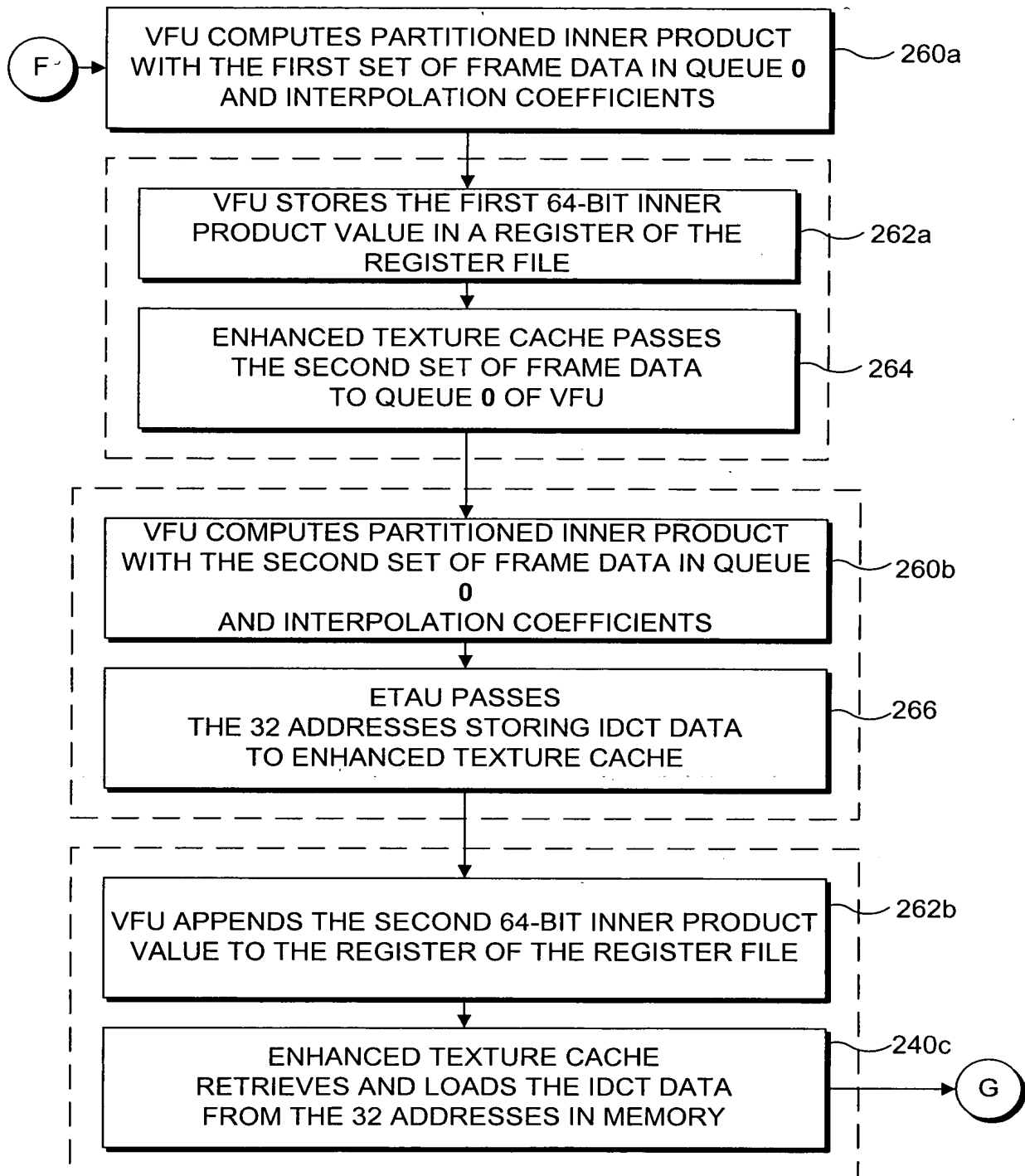


FIG. 11D

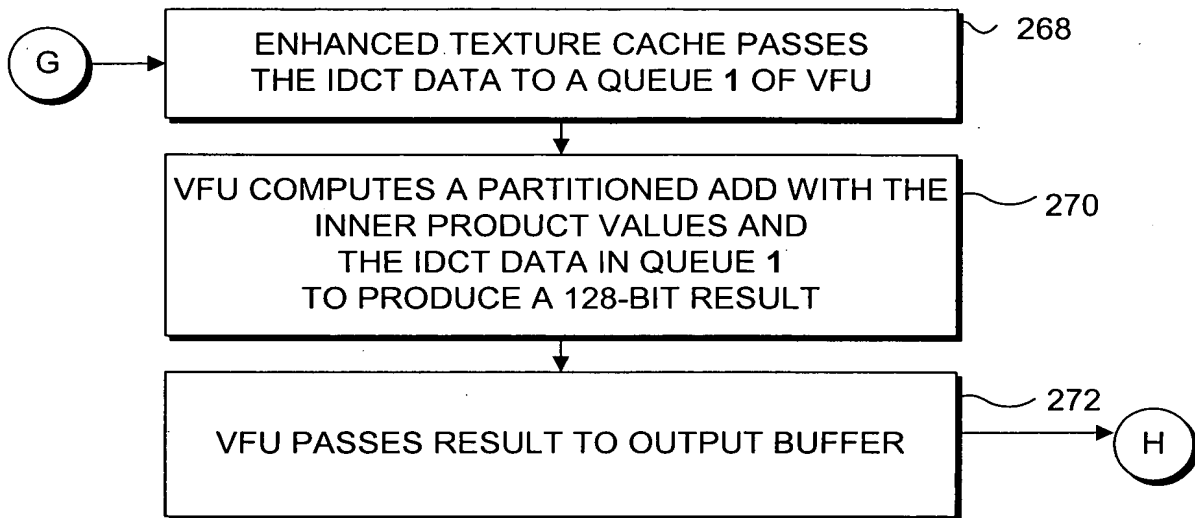


FIG. 11E

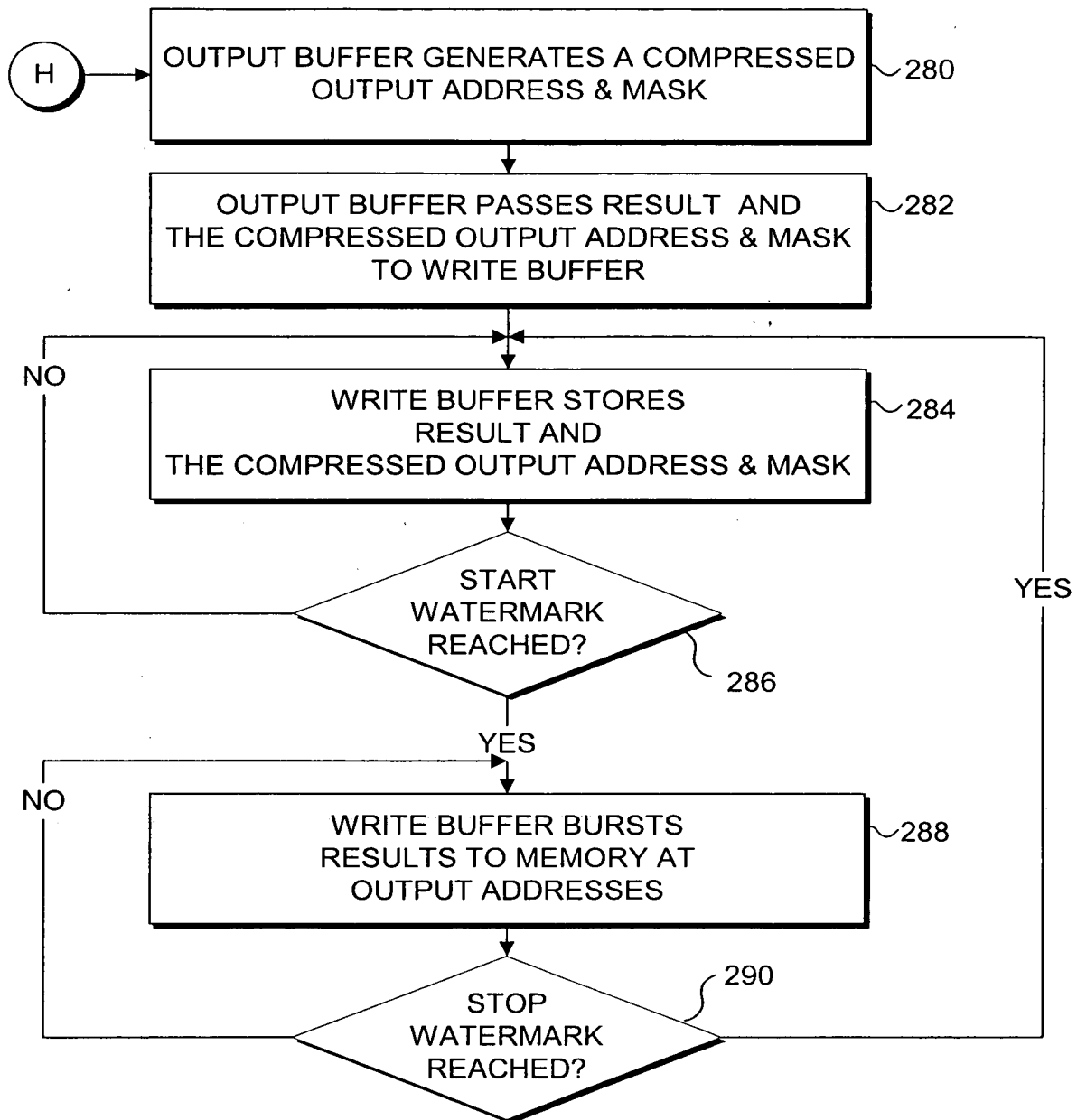


FIG. 11F